

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-15 are active in the present application. Claims 1-4 are amended and Claim 15 is added by the present amendment. Claims 6-14 are indicated as withdrawn in response to a previous restriction requirement.

Amendments to Claims 1-4 and new Claim 15 are supported by the originally filed claims and specification. Accordingly, no new matter is added.

In the outstanding Office Action, Claims 1 and 3 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,189,404 to Masimo et al. (herein "Masimo") in view of U.S. Patent No. 6,011,585 to Anderson; Claims 2 and 5 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 4,689,824 to Mitchell et al. (herein "Mitchell") in view of Anderson; and Claim 4 was indicated as allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claims.

Applicant gratefully acknowledges the Examiner's indication of allowable subject matter. Accordingly, Claim 4 is rewritten in independent form including all of the limitation of the base claim, Claim 3. Thus, it is respectfully submitted that amended Claim 4 is allowable.

Claims 1 and 3 were rejected under 35 U.S.C. § 103(a) as unpatentable over Masimo in view of Anderson. Applicant respectfully traverses that rejection with respect to amended Claims 1 and 3.

Amended Claim 1 is directed to a signal processing circuit in an image input apparatus that includes, *inter alia*, first and second storage sections provided with a plurality of storage regions of the same number of bits as the unit image signal. The storage regions of the first storage section and the storage regions of the second storage section are connected

such that an array of the unit image signal stored in a main memory is stored in the storage regions of the second storage section in a state of being rotated 90 degrees clockwise when the unit image signal stored in the main memory is transferred and stored in the storage regions of the first storage section, and then the unit image signal stored in the storage regions of the first storage section is transferred and stored in the storage regions of the second storage section.

In a non-limiting example, FIG. 2 shows register group RG2 (e.g., first storage section) and register group RG1 (e.g., second storage section). Further, as illustrated in the example of FIGs. 3(A), 3(B) and 3(C), an image array A-R (e.g., unit image signal) is stored in the register group RG1 (i.e., stored in storage regions of the second storage section) in a state of being rotated 90 degrees clockwise from the version stored in main memory, when the unit image signal stored in the main memory (e.g., FIG. 3(A)) is transferred and stored in RG2 (e.g., first storage section) and then transferred to RG1 (e.g., second storage section).

Applicant respectfully submits that Masimo does not teach or suggest a signal processing circuit in an image input apparatus that includes first and second storage sections connected such that a stored unit image signal is rotated 90 degrees clockwise when transferred and stored in the first storage section, and then transferred and stored in the second storage section. Applicant respectfully submits that Masimo only describes an arrangement of 1st through 4th registers 41a-41d (e.g., first storage section), respectively, connected to selector 42, FIG. 4B, which is not a storage device, but rather a multiplexing device without storage. Thus, the selector 42 has no “storage regions” as in Claim 1, and applicant respectfully traverses the assertion in the outstanding Office Action that Masimo’s selector 42 reads on the claimed second storage device.¹ Thus, Masimo describes a first storage section that is not connected to a second storage section, which is different than the

¹ Office Action at page 3, lines 6-12.

claimed invention. Hence, applicant respectfully submits that Masimo does not teach or suggest “storage regions of said first storage means and said storage regions of said second storage means are connected one another,” as in amended Claim 1.

In addition, Masimo indicates that message data is stored in a message BMM 11, passed through the circuit of FIG. 4B to be rotated, and then stored in rotated BMM 15.² Masimo also indicates that image data is stored in image BMM 19 and that image data is not rotated at all,³ which is different than the claimed invention. Thus, it is respectfully submitted that Masimo does not teach or suggest a “unit image signal . . . in a state of being rotated,” as in amended Claim 1.

Further, Masimo describes rotating message data in a counterclockwise direction to accommodate a rotating display device, in FIG. 3B, which is different than the claimed invention. Thus, it is respectfully submitted that Masimo also does not teach or suggest image data “stored . . . in a state of being rotated 90 degrees clockwise,” as in amended Claim 1.

Accordingly, applicant respectfully submits that amended independent Claim 1, and claims depending therefrom, patentably define over Masimo.

Claim 3 is directed to a signal processing circuit of an image input apparatus including, *inter alia*, first and second register groups. Storage regions in the first register group are connected directly to storage regions in the second register group.

In a non-limiting example, FIG. 2 shows a signal processing circuit including storage regions in register group RG1 (e.g., storage regions of a first register group) connected directly to storage regions in register group RG2 (e.g., storage regions of a second register group).

² Masimo at column 3, lines 58-64.

³ Masimo at column 2, lines 15-18, and at column 3, line 67, to column 4, line 2.

As discussed above, applicant respectfully submits that Masimo does not teach or suggest first and second register groups that are directly connected to each other. The selector 42 in FIG. 4B of Masimo does not include “storage regions” and thus may not be considered a “register group” having “registers” with “storage regions,” as in Claim 3.

Accordingly, it is submitted that Claim 3 also patentably defines over Masimo.

Further, applicant respectfully submits that Anderson also does not teach or suggest the features of Claims 1 and 3.

Accordingly, it is respectfully submitted that independent Claims 1 and 3, and claims depending therefrom, should be considered allowable.

Claims 2 and 5 were rejected under 35 U.S.C. 103(a) as unpatentable over Mitchell in view of Anderson.

Claim 2 is directed to a signal processing circuit in an image input apparatus including, *inter alia*, first and second storage sections that are directly connected one another by a predetermined connecting line, such that an array of a unit image signal stored in the storage regions of the first storage section is reflected about a centerline of the array, to be stored in the storage regions of the second storage section.

In a non-limiting example, Figures 4(A), 4(B) and 4(C) show an example of image data A-R (e.g., array of a unit image signal) that is reflected about a centerline of the array CL, when it is transferred from register group RG3 to register group RG2.

Applicant respectfully submits that Mitchell does not teach or suggest an apparatus configured to reflect data about a centerline. Further, applicant respectfully traverses the statement in the outstanding Office Action that Mitchell discloses “[w]hen the register groups are connected as shown in figure 4 of Mitchell, the image is reflected along its centerline.”⁴ FIG. 4 of Mitchell describes a method of rotating an image 180 degrees. As can be seen by

⁴ Office Action at page 6, lines 1-2.

comparing the illustrated “original image” and “rotated image,” the rotated image is not a reflected version of the original image, but instead is a version of the original image rotated 180 degrees. Further, the illustrated example of processing rows 2 and 5, in FIG. 4 of Mitchell also does not indicate that a reflected image is produced, but that data from two different rows are swapped, thereby indicating a swapping of data along two axes, which is different than a reflection about a centerline of an array. Hence, applicant respectfully submits that Mitchell does not teach or suggest that “an array of said unit image signal stored in said storage regions of said first storage section is reflected about a centerline of said array, to be stored in said storage regions of said second storage section,” as in Claim 2.

Accordingly, it is respectfully submitted that Claim 2 patentably defines over Mitchell.

Claim 5 is directed to a signal processing circuit of an image input apparatus, including second and third register groups with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in the image input apparatus and arranged in two dimensions. The second and third register groups have first to fourth registers, and the first to fourth registers have zero-th to third storage regions.

The zero-th to third storage regions of the first register of the second register group are connected directly, by a predetermined connecting line, to the third to zero-th storage regions of the first register of the third register group, respectively. The zero-th to third storage regions of the second register of the second register group are connected directly, by a predetermined connecting line, to the third to zero-th storage regions of the second register of the third register group, respectively. The zero-th to third storage regions of the third register of the second register group are connected directly, by a predetermined connecting line, to the third to zero-th storage regions of the third register of the third register group, respectively.

Further, the zero-th to third storage regions of the fourth register of the second register group are connected directly, by a predetermined connecting line, to the third to zero-th storage regions of the fourth register of the third register group, respectively.

In a non-limiting example, FIG. 2 shows a signal processing circuit of an image input apparatus including register group RG2 (e.g., second register group) and register group RG3 (e.g., third register group). Storage regions B0-B3 in register R1 of register group RG2 are connected to storage regions B3-B0, respectively, in register R1 of register group RG3. Further, B0-B3 in register R2 of register group RG2 are connected to storage regions B3-B0, respectively, in register R2 of register group RG3. Similar connections are found in registers R3 and R4 of register groups RG2 and RG3.

Thus, storage regions in each register of RG2, corresponding to a row in an image array, are connected to other storage regions in the corresponding register of RG3, corresponding to the same row in the image array.

Applicant respectfully submits that Mitchell does not teach or suggest connected register groups or alternatively any logical data connections, as in the claimed invention. Further, applicant respectfully traverses the indication in the outstanding Office Action that Mitchell discloses the claimed register connections.⁵ As discussed above, Mitchell discloses a method of rotating an image 180 degrees. Further, in FIG. 4, Mitchell shows a method of rotating an image that swaps data from different rows. For example, data in a second row (5, 6, 7, 8) is swapped with data in a fifth row (17, 18, 19, 20), which is different than the claimed connections in which registers of a same row are connected. Hence, it is respectfully submitted that Mitchell does not teach or suggest the claimed connections of Claim 5, including for example, “zero-th to third storage regions of said first register of said second

⁵ Office Action at page 6, line 20, to page 7, line 10.

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register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said first register of said third register group, respectively.”

Accordingly, it is submitted that Claim 5 also patentably defines over Mitchell.

Further, applicant respectfully submits that Anderson also does not teach or suggest the features of Claims 2 and 5.

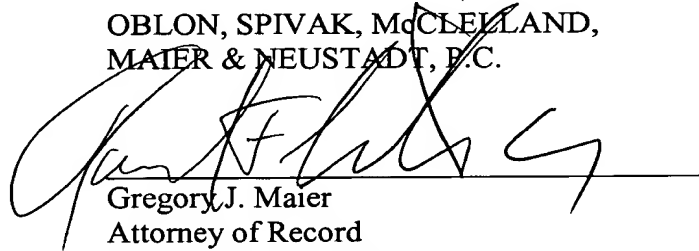
Accordingly, it is respectfully submitted that independent Claims 2 and 5 also be considered as allowable.

New Claim 15 depends on Claim 1 and is allowable for the same reasons.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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